CLMPTO

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TB

1. (Amended) A semiconductor wafer, including:

a plurality of the sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

[a plurality of chip electrodes positioned on said chip section; and]

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center.

2. (Original) A semiconductor wafer, including:

a plurality of chip sections defined theron by scribe lines,

each chip section having:

bump electrodes formed simultaneously theron; a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

said chip section having a center and a periphery and said interconnection layers extend from said periphery toward said center.

3. (Currently Amended) A semiconductor wafer including:

a plurality of chip sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes, wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein said aluminum layer and said plating extend from one of said bump electrodes to one of said chip electrodes and said plating contacts said one of said bump electrodes and said aluminum layer contacts said one of said chip electrodes.

4. (Currently Amended) A semiconductor wafer including:

a plurality of chip sections defined thereon by scribe lines, each chip section having: bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes, wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein said aluminum layer and said plating extends from one said bump electrodes to one of said chip electrodes and said plating contacts said one of said bump electrodes and said aluminum layer contacts said one of said chip electrodes.

5. (Original) A semiconductor wafer as in claim 3, wherein said plating compromises one of nickel and copper.

6. (Original) A semiconductor wafer as in claim 3, wherein said aluminum layer has a thickness of no greater than 1 micrometer.

7. (Original) A semiconductor wafer as in claim 3, wherein said plating has a thickness of at least 5 micrometers.

8. (Original) A semiconductor wafer as in claim 3, further comprising a gold layer between said bump electrode and said plating.

9. (Amended) A semiconductor wafer as in claim [1] 4, wherein each of said chip sections has a center and a periphery and said interconnection layers extend from said periphery toward said center.

10. (Original) A semiconductor wafer as in claim 4, wherein said plating comprises one of nickel and copper.

11. (Original) A semiconductor wafer as in claim 4, wherein said aluminum layer has a thickness of no greater than one micometer.

12 (Original) A semiconductor wafer as in claim 4, wherein said plating has a thickness of at least 5 micrometers.

CLAIMS 13-14 ARE CANCELLED

15. (New) The semiconductor wafer of claim 3, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

16. (New) The semiconductor wafer of claim 4, wherein each chip section has a center and a periphery and said interconnection layers extend from said periphery toward said center, and wherein the plurality of chip electrodes are positioned on said periphery.

CLAIMS17-24 ARE CANCELLED

25. (New) A semiconductor wafer of claim 1, wherein said bump electrodes are arranged in a grid array.

26. (New) The semiconductor wafer of claim 2, wherein said bump electrodes are arranged in a grid array.

27. (New) The semiconductor wafer of claim 3, wherein said bump electrodes are arranged in a grid array.

28. (New) The semiconductor wafer of claim 4, wherein said bump electrodes are arranged in a grid array.

29. (New) The semiconductor wafer of claim 1, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

30. (New) The semiconductor wafer of claim 2, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

31. (New) The semiconductor wafer of claim 3, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.

32. (New) The semiconductor wafer of claim 4, wherein a pitch of said chip electrodes is different from a pitch of said bump electrodes.